

AMENDMENTS TO THE CLAIMS

1-29 (Cancelled)

30. (Currently Amended) An apparatus comprising:
an operating system to request a chip to start a time counter prior to entering a
reduced power consumption state, wherein the chip is further to store a
time of entering the reduced power consumption state and a time of
exiting the reduced power consumption state; and
the chip to start the time counter, wherein the chip is further to automatically
calculate a reduced power consumption state duration.
31. (Original) The apparatus of claim 30 wherein the operating system further
operates to request the chip to halt the time counter.
32. (Original) The apparatus of claim 30 wherein the chip further operates to halt
the time counter.
33. (Original) The apparatus of claim 30 wherein the time counter comprises a
reduced power consumption state duration.
34. (Currently Amended) The apparatus of claim 30 wherein the chip ~~is~~ comprises a
personal computer chipset.
35. - 56. (Cancelled)
57. (Currently Amended) A method comprising:
storing a time of entering a reduced power consumption state in a chip, wherein
the chip is further to start a time counter prior to entering a reduced power
consumption state;
storing a time of exiting the reduced power consumption state in the chip prior to
an execution of an interrupt routine; and

automatically calculating a reduced power consumption state duration.

58. (Previously Presented) The method of claim 57 wherein the storing the time of entering the reduced power consumption state comprises storing the time of entering in a register.
59. (Previously Presented) The method of claim 57 wherein the storing the time of exiting the reduced power consumption state comprises storing the time of exiting in a register.
60. (Previously Presented) The method of claim 57 wherein the automatically calculating the reduced power consumption state duration is performed by the chip.
61. (Previously Presented) The method of claim 60 wherein the chip is a personal computer chipset.
62. (Cancelled)
63. (New) A system comprising:
a server having a chipset coupled with a central processing unit further coupled with a storage medium, wherein the central processing unit having an operating system to request a chip to start a time counter prior to entering a reduced power consumption state, wherein the chip is further to store a time of entering the reduced power consumption state and a time of exiting the reduced power consumption state; and
the chipset having the chip to start the time counter, wherein the chip is further to automatically calculate a reduced power consumption state duration.
64. (New) The system of claim 63 wherein the operating system further operates to request the chip to halt the time counter.

65. (New) The system of claim 63 wherein the chip further operates to halt the time counter.
66. (New) The system of claim 63 wherein the time counter comprises a reduced power consumption state duration.
67. (New) The system of claim 63 wherein the chip comprises a personal computer chipset.